PaRSEC ENABLED LIBRARIES AND APPLICATIONS

The Distributed Tasking for Exascale (DTE) project extends the capabilities of ICL’s Parallel Runtime and Execution Controller (PaRSEC) project—a generic framework for architecture-aware scheduling and management of microtasks on distributed, many-core, heterogeneous architectures. The PaRSEC environment also provides a runtime component for dynamically executing tasks on heterogeneous distributed systems along with a productivity toolbox and development framework that supports multiple domain-specific languages and extensions and tools for debugging, trace collection, and analysis.

High level DAG, Cholesky factorization

Dependencies are expressed between block columns of the matrix

High level tasks insert tile-level tasks, synchronize, or insert (a)synchronous communication tasks

### ECP SLATE

**Cholesky Factorization (POTRF)**

- **Double Precision** - 64 cores, 1 to 4 V100
- **Tiles of 1024x1024 doubles**

### DPLASMA

**Hybrid Matrix-Matrix Multiply (GEMM)**

- **Double precision** (double) / 272 Nodes of Summit (40 cores + 8 V100s)
- **Tiled Algorithm, with tiles of 1024x1024 doubles**

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**Massively Parallel Quantum Chemistry (MPQC)**

- Application part of NWChemEx
- Base implementation on top of TiledArray, itself programmed on top of MADNESS
- Replace tensor ‘ABCD’ tensor contraction in TA with a PaRSEC native implementation
- Use MADNESS over PaRSEC to simplify sharing of resources between MPQC/TA and PaRSEC native code

\[
R_{ab}^{cd} = \sum_{cd} T_{cd}^{ij} V_{ab}^{cd}
\]

### Synthetic Benchmark

(random matrices)

**Applicative case (C65H132)** on Hybrid System

**HiCMA Hierarchical Computations on Manycore Architectures**

**Tile, Low-Rank, Cholesky Factorization for Large Matrices**

- Shaheen II: 4096 nodes (32 cores each @ 2.30 GHz (Intel Haswell))

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Find out more at http://icl.utk.edu/dte/