PAPI (Performance Application Programming Interface) provides a consistent interface (and methodology) for hardware performance counters found across a compute system: i.e., CPUs, GPUs, on- and off-chip memory, interconnects, I/O system, file system, energy/power, etc. PAPI enables software engineers to see, in near real time, the relationship between software performance and hardware events across the entire compute system.

**STANDARD FEATURES**
- Standardized Performance Metrics
- Easy Access to Platform-Specific Metrics
- Multiplexed Event Measurement
- Dispatch on Overflow
- Overflow & Profiling on Multiple Simultaneous Events
- Bindings for C, Fortran and Matlab
- User Definable Metrics derived from Platform-Specific Metrics
- Support for Virtual Computing Environments
- Performance Counter Monitoring at Task Granularity for Dataflow Runtime PaRSEC

**SUPPORTED ARCHITECTURES**
- **AMD**
  - X86
- **ARM**
  - Cortex A7, A8, A9, A15, X-Gene (ARM64), Raspberry Pi
- **CRAY**
  - Gemini and Aries interconnects
  - RAPO power
- **IBM**
  - Blue Gene Series
  - Q: 6D-Torus, I/O system
  - EMON power on BG/Q
  - Power Series
  - PCP-support for POWER9
- **Infiniband**
  - Nehalem, Westmere, Sandy Bridge, Ivy Bridge, Haswell, Haswell-EP, Broadwell, Skylake-X
  - Kaby Lake, Knights Corner, Knights Landing, Knights Mill
  - RAPO; power capping, Power on Xeon Phi
  - Intel RAPL (power/energy), power capping capabilities (via PAPI_write())
- **Lustre**
  - Tesla, Kepler, Maxwell, Pascal, Volta
  - support for multiple GPUs
  - NVIDIA GPU support for power/energy reading; power capping capabilities (NVML)
- **Virtual Environment**
  - VMware, KVM

**FutureGrid** provided resources for testing and development of PAPI-V

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http://icl.utk.edu/papi
PAPI provides tool designers and application engineers with a consistent interface and methodology for the use of low-level performance counter hardware found across the entire compute system (i.e. CPUs, GPUs, on/off-chip memory, interconnects, I/O system, energy/power, etc.). PAPI enables users to see, in near real time, the relationships between software performance and hardware events across the entire compute system.

Exa-PAPI builds on the latest PAPI project and we will extend it with:

• Performance counter monitoring capabilities for new and advanced ECP hardware, and also software technologies;
• Fine-grained power management support;
• Integration capabilities for exascale paradigms, such as task-based runtime systems that support dataflow programming models;
• “Software-defined Events” that originate from the ECP software stack and are currently treated as black boxes (i.e., communication libraries, math libraries, task-based runtime systems, etc.).

The objective is to enable monitoring of both types of performance events—hardware- and software-related—in a uniform way, through one consistent PAPI interface. That implies 3rd-party tools and application developers have to handle only a single hook to PAPI in order to access all hardware performance counters in a system, including the new software-defined events.

**EXASCALE COMPUTING PROJECT**

Exa-PAPI is part of ICL’s involvement in the Exascale Computing Project (ECP). The ECP was established with the goals of maximizing the benefits of high-performance computing (HPC) for the United States and accelerating the development of a capable exascale computing ecosystem. Exascale refers to computing systems at least 50 times faster than the nation’s most powerful supercomputers in use today.

**PUBLICATIONS**


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