Intel Core Architecture
An Analysis of the Haswell and Ivy Bridge Architectures by Intel

by

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Abstract

Every year Intel releases a new set of processors on the scene, with a list of improvements over the previous generation. This time around, it's the fourth-generation Intel Core processors (codenamed Haswell). The new generation does not necessarily render the older generation i.e. third generation (codenamed Ivy Bridge) obsolete. The focus of this report is to analyse and present how much the fourth generation of Intel processors have improved over the third generation processors as well as where it lags behind.

This report gives an analysis and comparison between the Ivy Bridge and Haswell architectures of Intel. We have tried to make a comparison between the two Intel architectures based on cache performance, power consumption, instruction sets, overall performance, branch prediction, the execution units of the architectures and finally, a price/performance ratio.
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Chapter 1
Cache Performance

The load and store bandwidth doubles for Haswell compared to Ivy Bridge. The TLB (Translation Look-aside Buffer) is also significantly improved in Haswell. The Haswell processor has the same number of dedicated pages but also has access to 2M shared pages. The page entry doubled in Haswell as well as the associativity i.e. Ivy Bridge had a 4-way associative TLB whereas Haswell has a 8-way associative TLB. The following table summarizes the changes.

<table>
<thead>
<tr>
<th>Metric</th>
<th>Ivy Bridge</th>
<th>Haswell</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 Load Bandwidth</td>
<td>32 Bytes/cycle</td>
<td>64 Bytes/cycle</td>
</tr>
<tr>
<td>Store Bandwidth</td>
<td>16 Bytes/cycle</td>
<td>32 Bytes/cycle</td>
</tr>
<tr>
<td>L2 Bandwidth to L1</td>
<td>32 Bytes/cycle</td>
<td>64 Bytes/cycle</td>
</tr>
<tr>
<td>L2 Unified TLB</td>
<td>4K: 512, 4-way</td>
<td>4K+2M shared:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1024, 8-way</td>
</tr>
</tbody>
</table>

The overall cache performance of the Haswell processor is better than the Ivy Bridge. The L1 cache has a 84.16% increase, L2 cache has a 7.21% increase and L3 cache has a 3% decrease in bandwidth in Haswell than in Ivy Bridge.
Chapter 2

Power Consumption

The Ivy Bridge consumes less power than Haswell. However, in idle state the Haswell consumes less power. The figure below does a comparison between the i5 Haswell and i7 Ivy Bridge and i7 Haswell. In the idle stage i7 Ivy Bridge consumes the highest power. The i5 Haswell and the i7 Haswell has similar power consumption in idle state

One of the biggest additions in Haswell is the full integration of the voltage regulator onto the CPU die. Instead of relying on the motherboard to produce a variety of power rails for different parts of the chip (memory controller, PCIe controller, GPU), Haswell has a fully-integrated voltage regulator (FIVR) that takes a single input (~1.8V) and splits it into all the required rails. The end result is an overall reduction in system power (~20%), comparable idle CPU/GPU power, but a sizable increase in load power consumption (~10%).

This obviously makes Haswell ideal for mobile computing, where there’s a lot of idling and puttering around the interwebs. These power savings are so extensive that they could equate to a 25% battery life improvement over Ivy Bridge. On the desktop, though, where you might be playing games, editing photos, or encoding videos, Haswell only just scrapes a victory from Ivy Bridge.
Chapter 3
Instruction Sets

The Intel Haswell processor includes AVX2 and FMA3 instructions, that were introduced in the recent past. Even though these extensions are not extensively supported by applications yet, their support should improve in future programs.

AVX2 is an expansion of the new AVX instruction set introduced with Sandy Bridge. The most important element of AVX was that Intel had improved the floating point units of the processor so they could process 256-bit numbers. AVX came with 12 new instructions, some of which are suitable for three variables. For example, it included an instructions for \( C = A + B \). Prior to AVX, processor could only work with two variables, so the above equation had to go: \( A = A + B \), and then \( C = A \).

AVX2 takes this a step further. An important improvement in Haswell is that the integer execution units now can work with 256-bit numbers. The number of instructions that can work with three variables has been increased, including instructions for multiplications and bit operations. There are new instructions for retrieving data according to the gather-scatter method, which is important for vector calculations used by multimedia software.

AVX2 also has something that was on many developers' wishlists, called Fused Multiply-Add (FMA). It allows numbers to be multiplied and added in one operation. AMD already introduced an FMA instructions with the Bulldozer core, but they aren't compatible with each other. Intel went with FMA3, with a maximum of three variables, \( (C = A \times B + C) \). Intel's simpler version can still improve performance quite a bit for AVX2-compiled software.
The CineBench Benchmark is three years old and is not optimized for AVX. The above chart gives us more insight on how two processors would perform with older applications which may not have been optimized with AVX. Without any optimizations using the new instruction set that Haswell supports, Ivy Bridge performs 7% less than Haswell in Single-Thread and 10% less in Multi-Thread. Considering the absence of any optimizations, this is a significant improvement in Haswell.

The SiSoft Sandra benchmarks can be used to measure multimedia performance with or without the FMA3 and AVX2 instruction sets (which are the new inclusions in Haswell). The following chart shows the performance of Haswell compared to Ivy Bridge. The performance of the Haswell processors are shown with and without the FMA3 and AVX2 instruction sets.
The Haswell processor performs significantly better with FMA3 and AVX2 than Ivy Bridge which does not support the AVX2 instruction set.
Chapter 5
Execution Units

The two instruction decode queue in Ivy Bridge has been merged into one in Haswell. The reorder buffer has been enlarged from 168 entries in Ivy Bridge to 192 in Haswell. Two new ports 6 and 7 were added to improve load balancing and parallelization. These new ports are connected to the functional unit that does integer computations. Initially, in Ivy Bridge, there were two ports with the functional units dedicated to both vectors and integer computations. The Haswell improves performance by having ports with functional units dedicated to integer computations.
The above diagram shows the execution units for the Haswell processor.
Chapter 6  
Branch Prediction

The following table gives difference between Ivy Bridge and Haswell

<table>
<thead>
<tr>
<th></th>
<th>IvyBridge</th>
<th>Haswell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Misprediction penalty</td>
<td>15 clock cycles or more for branches inside the µop cache and slightly more for branches in the level-1 code cache</td>
<td>It was measured to 15 - 20 clock cycles. Varies a lot</td>
</tr>
<tr>
<td>Pattern recognition for</td>
<td>Nested loops and loops with branches inside are not predicted particularly well</td>
<td>Loops are successfully predicted up to a count of 32 or a little more. Nested loops and branches inside loops are predicted reasonably well</td>
</tr>
<tr>
<td>conditional jumps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pattern recognition for</td>
<td>Indirect jumps and indirect calls (but not returns) are predicted using the same two-level predictor as branch instructions</td>
<td>Indirect jumps and indirect calls are predicted well</td>
</tr>
<tr>
<td>indirect jumps and calls</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BTB organization</td>
<td>Unknown. It can handle a maximum of four call instructions per 16 bytes of code. Conditional jumps are less efficient if there are more than 3 branch instructions per 16 bytes of code</td>
<td>Unknown but it appears to be reasonably big</td>
</tr>
<tr>
<td>Prediction of function returns</td>
<td>The return stack buffer has 16 entries for near returns</td>
<td>The return stack buffer has 16 entries for near returns</td>
</tr>
</tbody>
</table>

µop cache: only stores **decoded** instructions.  
L1: stores regular x86 instructions.  
BTB: Branch target Buffer.
Chapter 7
Price/Performance Ratio

Ivy Bridge has a better price/performance ratio than Haswell. The performance of the Haswell processor is better than that of Ivy Bridge but the cost is disproportionately higher.
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